WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a semiconductor substrate;

dummy patterns for a chemical mechanical polishing (CMP) method formed in a uniform pattern over the semiconductor substrate; and

marking patterns that are formed over the semiconductor substrate to correspond to predetermined groups of the dummy patterns.

2. The semiconductor device of claim 1, wherein the marking patterns have a different shape from the dummy patterns.

3. The semiconductor device of claim 1, wherein the marking patterns have a different size from the dummy patterns.

4. The semiconductor device of claim 1, wherein the marking patterns are smaller than the dummy patterns.

5. A semiconductor device comprising:

a semiconductor substrate;

dummy patterns for a CMP method formed in a uniform pattern over the semiconductor substrate; and

marking lines that divide the dummy patterns into a plurality of groups.

6. The semiconductor device of claim 5, wherein the marking lines are formed of marking patterns that have a different shape from the dummy patterns and surround the groups of dummy patterns.

7. The semiconductor device of claim 5, wherein the marking lines are formed of marking patterns that have a different shape from the dummy patterns and form a grid pattern.

8. The semiconductor device of claim 5, wherein the marking lines are formed of marking patterns that have a different size from the dummy patterns and surround the groups of dummy patterns.

9. The semiconductor device of claim 5, wherein the marking lines are formed of marking patterns that have a different size from the dummy patterns and form a grid pattern.

10. The semiconductor device of claim 5, wherein the marking lines are formed of marking patterns that are smaller than the dummy patterns and surround the groups of dummy patterns.

11. The semiconductor device of claim 5, wherein the marking lines are formed of marking patterns that are smaller than the dummy patterns and form a grid pattern.

12. A semiconductor device comprising:

a semiconductor substrate;

a reference plain that covers the semiconductor substrate; and

marking lines that divide the reference plain into a plurality of groups.

13. The semiconductor device of claim 12, wherein the marking lines are provided in the reference plain.

14. The semiconductor device of claim 13, wherein the plurality of groups are electrically connected to one another.

15. The semiconductor device of claim 12, wherein the marking lines form a grid.

16. The semiconductor device of claim 12, wherein each group has a different shape and size.

17. A method of locating a predetermined point on a semiconductor device, the semiconductor device comprising a semiconductor substrate, dummy patterns for a chemical mechanical polishing (CMP) method formed in a uniform pattern over the semiconductor substrate, and marking patterns that are formed over the semiconductor substrate to correspond to predetermined groups of the dummy patterns, the method comprising:

counting a number of the marking patterns from a first marking pattern closest to a reference point to a second marking pattern closest to the predetermined point; and

counting a number of the dummy patterns from a first dummy pattern closest to the second marking pattern to a second dummy pattern closest to the predetermined point.

18. The method of claim 17, wherein the marking patterns have a different size from the dummy patterns.

19. The method of claim 17, wherein the marking patterns are smaller than the dummy patterns.

20. A method of locating a predetermined point on a semiconductor device, the semiconductor device comprising a semiconductor substrate, a reference plain that covers the semiconductor substrate, the reference plain comprising a plurality of via holes, and marking lines that divide the reference plain into a plurality of groups of the via holes, the method comprising:

counting a number of the marking lines from a first marking line closest to a reference point to a second marking line closest to the predetermined point; and

counting a number of the via holes from a first via hole closest to the second marking line to a second via hole closest to the predetermined point.

21. The method of claim 20, wherein the marking lines form a grid.

22. The method of claim 20, wherein each group has a different shape and size.